REMARKS

The final Office Action dated October 20, 2008, and the patents and publications relied on therein have been carefully reviewed, and in view of the following remarks reconsideration and allowance of all the claims pending in the application are respectfully requested.

Claim 7 stands rejected. By this Response, claim 7 has been amended and remains pending.

The Amendment Of Claim 7

Claim 7 has been amended to improve its form in accordance with U.S. patent law. In particular, the phrase "one of" has been deleted in line 10, thereby removing an inadvertent typographical error. Applicants respectfully submit that the amendment to claim 7 should be entered at this stage of prosecution because the amendment does not raise issues that would require further consideration and/or search.

The Rejection Under 35 U.S.C. § 103(a) Over Jolitz In View Of Connery And Follett et al.

Claim 7 stands finally rejected under 35 U.S.C. § 103(a) as unpatentable over Jolitz, U.S. Patent Application Publication No. 2001/0025315 A1, in view of Connery et al. (Connery), U.S. Patent No. 6,570,884 B1, and Follett et al. (Follett), U.S. Patent No. 6,094,712.

Applicants respectfully traverse this rejection. Applicants respectfully submit that the subject matter according to claim 7 is patentable over Jolitz in view of Connery and Follett. Applicants respectfully submit that even if Jolitz, Connery and Follett are properly combinable, the resulting method is not the subject matter of claim 7. More specifically, none of Jolitz, Connery or Follett discloses or suggests a method comprising initiating direct data placement of data associated with the application packet header when a result of masking a set of values corresponding to a direct data placement pattern with contents of the loaded registers matches at least one claimed direct data placement pattern. Additionally, none of Jolitz, Connery or Follett discloses or suggests a method comprising mapping a payload of the detected applications header to a memory based on the claimed direct data placement pattern, such that the claimed memory is a predetermined region of memory reserved for the application.

Regarding initiating direct placement of data, the Examiner asserts that paragraphs [0076] and [0075] of Jolitz discloses initiating direct data placement. (See final Office Action, page 3,

lines 3-10.) To the contrary, Applicants respectfully submit that paragraphs [0075] and [0076] of Jolitz disclose that the Rx engine compares a number of fields of the IP headers with expected values stored in a plurality of registers in Variable Content Addressable Memory (VxCAM) 22 to determine to which session an incoming IP datagram belongs. Certain fields in the TCP/IP headers are static and can be compared against static values. Other fields in the TCP/IP headers are variable and are compared against values stored in registers and predetermined values stored in ADE memory 56. Accordingly, nothing in paragraphs [0075] and [0076] of Jolitz relates to initiating direct data placement as asserted by the Examiner.

Once Jolitz determines the session to which an incoming IP datagram belongs, Rx engine 48 directly delivers a TCP payload to dual-port application memory 24. (See Jolitz, paragraph [0044], lines 7-8.) Jolitz discloses in paragraph [0045] that memory 24 contains the host system view of network memory, and a shadowed copy for the network accelerator to use for TCP segment transmission and reception. Jolitz further discloses that the host system software driver swaps application memory (system RAM) for memory 24, thereby allowing the host system direct access the network data stored in the dual-port/double banked memory and effectively replacing the role of host system RAM. (See Jolitz, paragraph [0045], lines 1-8.) Thus, because the Jolitz host system software swaps application memory for memory 24 and uses memory 24 in a way that effectively replaces the role of the host system RAM, it follows that Jolitz does not disclose or suggest initiating direct data placement of data. Moreover, because Jolitz does not disclose or suggest initiating direct data placement of data, it follows that none of the registers in Jolitz VxCAM 22 disclose or suggest the claimed at least one direct data placement pattern.

Further still, because the Jolitz host system software swaps application memory for memory 24 and uses memory 24 in a way that effectively replaces the role of the host system RAM, it follows that Jolitz does not disclose or suggest that memory 24 is reserved for an application or that Jolitz maps a payload of a detected application header based on a direct data placement pattern into the claimed memory that is a predetermined region of memory reserved for the application.

Regarding Connery, Connery discloses that incoming data is supplied to the receive FIFO 201, and from receive FIFO 201 on line 202 to the host port. (See Connery, column 5, lines 39-42, and Figure 3.) Thus, Connery discloses or suggests nothing regarding initiating

direct data placement of data or the claimed at least one direct data placement pattern. Further, Connery does not disclose or suggest the claimed memory that is a predetermined region of memory reserved for claimed application. Consequently, Connery cannot disclose or suggest mapping a payload of the detected application header to a memory based on the direct data placement pattern, such that the memory is a predetermined region of memory reserved for the application.

Regarding Follett, Applicants respectfully submit that the Examiner's characterization of Follett ignores the fact that Follett discloses a dynamic buffer 120 that is used for buffering incoming data before the data is transferred to the memory associated with an application. More specifically, Follett discloses an interface unit 54 that includes, among other components, a Virtual Circuit Identifier (VCI) memory map 95, a dynamic buffer memory 120 and a parser 139. VCI memory map 95 stores a map of the virtual addresses provided by an application 60 to the corresponding physical memory addresses in a main memory 44.[1] According to Follett, incoming data is loaded into buffer memory 120 when the incoming data is received. (See Follett, column 5, lines 18-21.) A parser 139 interprets the header of each ATM cell of the incoming data and causes a data portion of each ATM cell to be loaded into buffer memory 120. The incoming data is loaded into space within buffer memory 120 that is indexed by the VCI identified in the header of the ATM cell. (See Follett, column 5, lines 28-38.) Subsequently, the data is retrieved from buffer memory 120 and transferred to specific physical memory locations in main memory 44, as identified in VCI memory map 95. (See Follett, column 6, lines 18-24, and column 7, lines 6-12.)

According to Follett, each writing operation into buffer memory 120 is generally followed by a reading operation in which information is retrieved from buffer memory 120. Higher priority reads are recognized first, followed by lower priority retrievals. Variable blocks

[1] It is respectfully noted that at column 4, line 26, Follett makes reference to corresponding physical references in a memory 55; however, no memory 55 is depicted in any of the Figures of Follett. Instead, Figure 1B depicts a network interface unit 55 that is part of a disk server 35. It is also respectfully noted that Follett makes reference to application programs 48 that are contained in a main memory 44. (See Follett, column 2, lines 54-56.) But, Figure 1A depicts applications 60 that are contained in main memory 44 and column 4, lines 12-16, of Follett disclose an application 60 within main memory 44. Thus, Applicants respectfully submit that one of skill in the art (for whom the Follett specification was written) would conclude that the reference to application program 48 should be correctly interpreted as a reference to applications 60, and that an application 60 is contained in main memory 44. (Also see Follett, column 3, lines 55-65.) Further, Applicants respectfully submit that the reference to a memory 55 at column 4, line 26, of Follett would be interpreted by one of skill in the art to actually be a reference to memory 44.

of data are transferred from buffer memory 120 to the host computer to optimize latency. When buffer memory 120 begins to saturate, larger blocks of data are transferred to the host computer, thereby optimizing transfer efficiency and preventing memory overload. Follett discloses that transferring larger blocks of data to the host computer ordinarily occurs as a result of host saturation so that access to the system bus is temporarily limited. (See Follett, column 7, lines 23-40.) Thus, retrieval of data from buffer memory 120 to the host computer is initiated based on a priority level of the incoming data and a latency optimization to prevent memory overload, and is not initiated based on a direct data placement pattern.

Thus, Applicants respectfully submit that Follett does not disclose or suggest a method comprising initiating direct data placement of data associated with the application packet header when a result of masking a set of values corresponding to a direct data placement pattern with contents of the loaded registers matches the claimed at least one direct data placement pattern. Further, Applicants respectfully submit that Follett does not disclose or suggest a method comprising mapping a payload of the detected applications header to a memory based on the claimed direct data placement pattern, such that the claimed memory is a predetermined region of memory reserved for the application.

Accordingly, Applicants respectfully submit that the method resulting from the combination of Jolitz, Connery and Follett is not the claimed subject matter, and that claim 7 is patentable over Jolitz in view of Connery and Follett.

Consequently, Applicants respectfully request that the Examiner withdraw this rejection and allow claim 7.

Applicants notes that additional patentable distinctions between Jolitz, Connery and Follett and rejected claim 7 exist; however, the foregoing is believed sufficient to address the Examiner's rejections. Additionally, failure of Applicants to respond to a position taken by the Examiner is not an indication of acceptance or acquiescence of the Examiner's position. Instead, it is believed that the Examiner's positions are rendered moot by the foregoing and, therefore, it is believed not necessary to respond to every position taken by the Examiner with which Applicants do not agree.

CONCLUSION

In view of the above amendments and arguments which present the claims in better form for consideration on appeal, it is urged that the present application is now in condition for allowance. Should the Examiner find that a telephonic or personal interview would expedite passage to issue of the present application, the Examiner is encouraged to contact the undersigned attorney at the telephone number indicated below.

It is requested that this application be passed to issue with claim 7.

Respectfully submitted,

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